Non-Blocking Ruggedized Ethernet Switch (NRES)

Intelligent Automation, Inc.

23nd Test Instrumentation Workshop

Las Vegas
May 16th, 2019

This project is funded by the Test Resource Management Center (TRMC) Test and Evaluation/Science & Technology (T&E/S&T) Program through the U.S. Army Program Executive Office for Simulation, Training, and Instrumentation (PEO STRI) under Contract No. W900KK-13-C-0023. The Executing Agent and Program Manager work out of the AFTC.

Problem Statement

The Need

- Flight test instruments on a test article use Ethernet for interconnection.
- Current managed ruggedized Ethernet switches do not support fiber ports at 10Gbps speed, and guarantee non-blocking functionality at the same time.

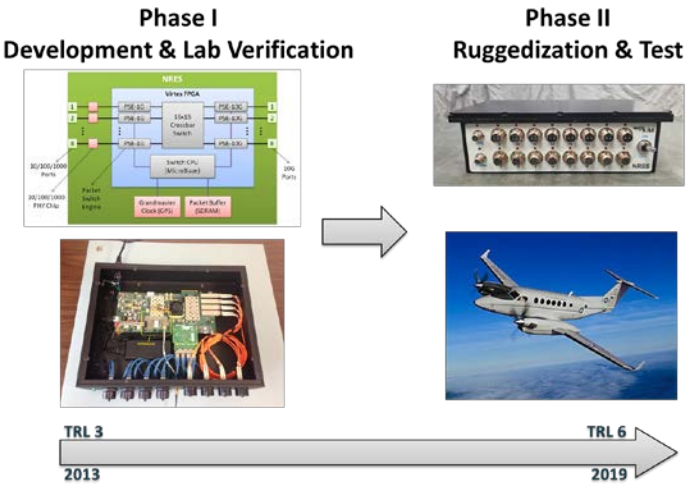
The Challenges

- Handling of multiple Ethernet ports at 10Gbps in a ruggedized switch.
- Support for several non-blocking ports.
- Support for time synchronization protocol (IEEE 1588)
- Support for management functions.

Description

- **Phase I**
  - Define Requirements and Specifications
  - Design and develop an eight port switch breadboard system for proof-of-concept
  - Demonstrate non-blocking 10Gbps operation in lab
- **Phase II**
  - Develop a 16 port ruggedized switch
  - Implement all required Layer 2/3 protocols including IEEE 1588
  - Test hardware to verify MIL-STD-810G compliance

TRL Progression



State-of-the-Art

- Current ruggedized Ethernet switches lack one or more of the following features:
  - Support for 10G ports.
  - Guarantee true non-blocking.
  - Management support through SNMP.
  - Support for time synchronization (IEEE 1588).
- Example manufacturers:
  - OnTime Networks
  - Curtiss-Wright
  - Amphenol-Socapex
  - Aitech
  - …

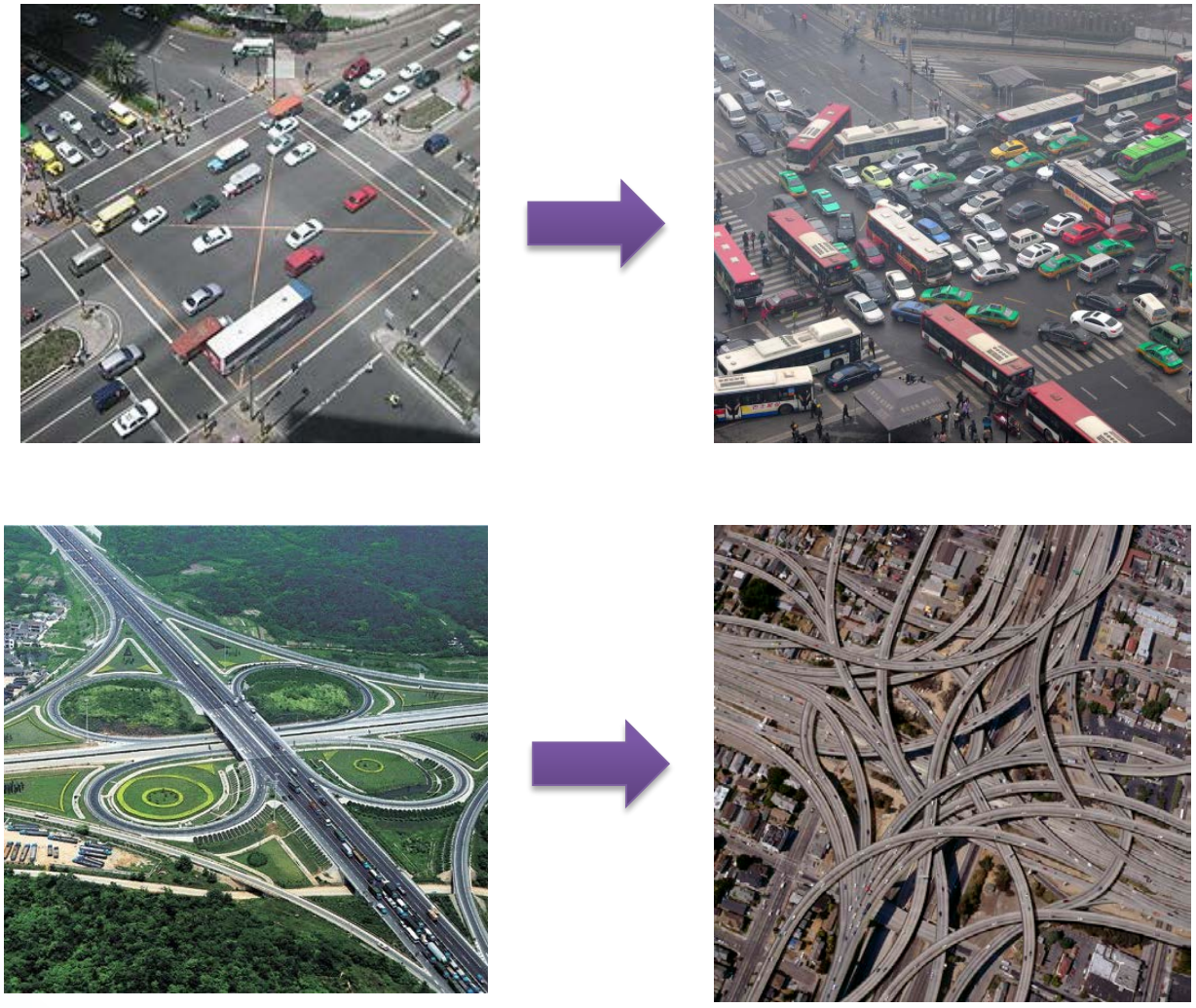
Objectives

- The primary objective of Phase I was to develop a prototype Ethernet switch on COTS hardware that supports four 10/100/1000 ports and four 10G ports and is non-blocking.
- The primary objective of the Phase II program is to bring the prototype developed in Phase I to a maturity level of TRL 6. This would involve:
  - Develop and test of a ruggedized board suitable for airborne applications.
  - Import all Phase I FPGA developments into this new board and finalize them.
  - Increase number of ports to eight 10/100/1000 ports and eight 10G ports.

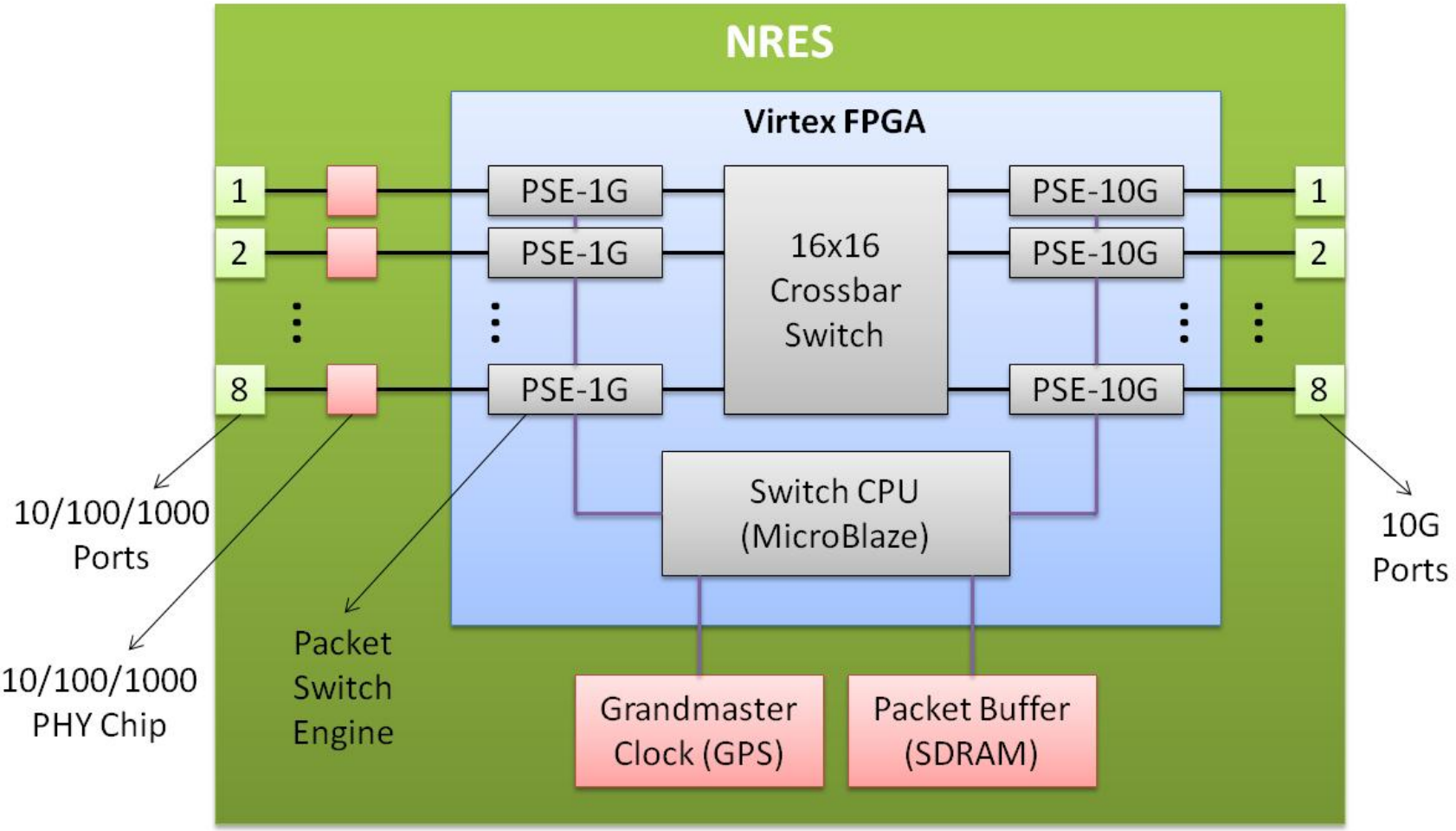
IRIG/TmNS Standards Utilized by NRES

- Physical Layer:
  - Wired Ethernet 10/100/1000 (copper) and 10G (fiber)
- Data Link Layer: fully supported
  - Examples: MAC and LLC
- Internet Layer: fully supported
  - Examples: IPv4, IPv6, ICMP and IGMP
- Transport Layer: fully supported
  - Examples: TCP and UDP
- Application Layer:
  - Management: SNMP (partial MIB)
  - Time Synchronization: IEEE 1588-2008 (grandmaster)
- Quality of Service: fully supported
  - Examples: DiffServ

Blocking vs Non-Blocking

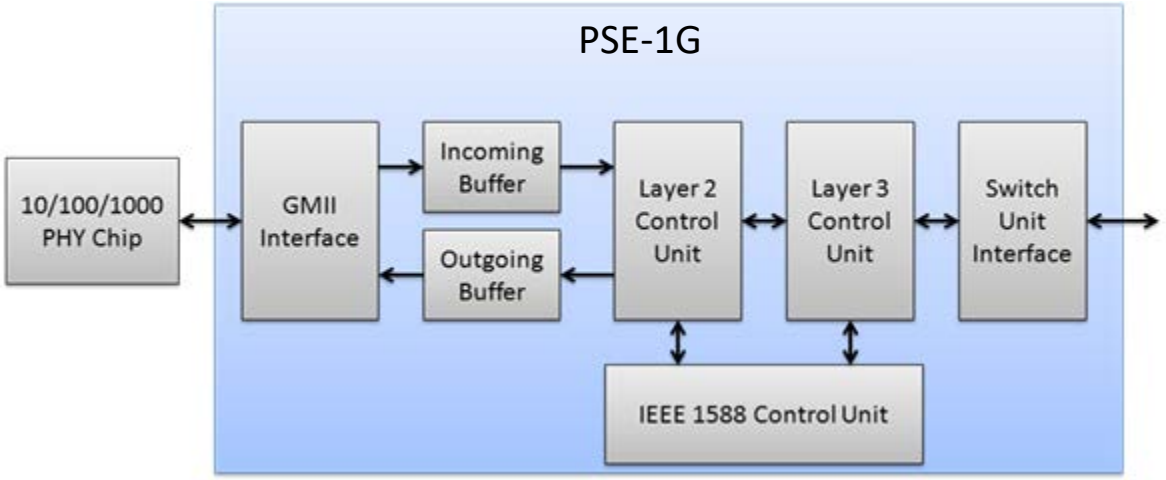


NRES Block Diagram



Packet Switch Engine

- Processing unit per port with allocated resources.
- CAM based lookup for line rate processing.
  - On-chip RAM blocks utilized as CAM modules.
- Multiple parallel buffers to support QoS.
- Hardware-based layer 2 and layer 3 switching
  - CPU not involved in the actual packet switching process

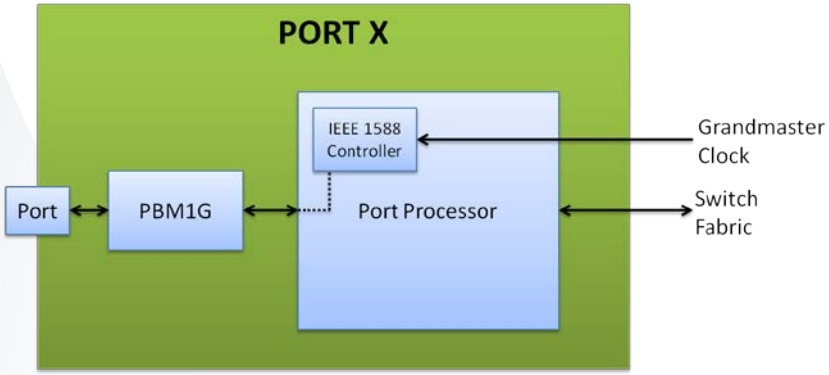


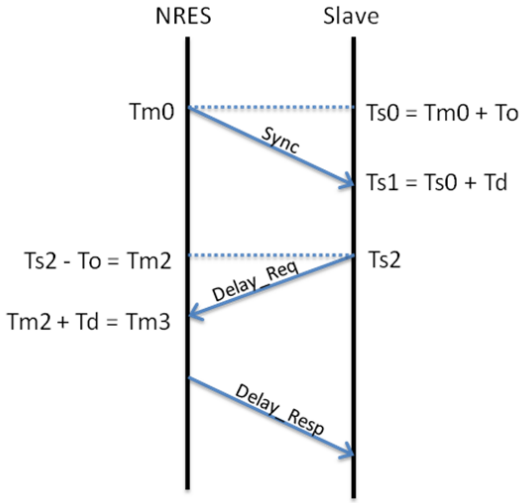
Switch CPU

- Soft-core Microblaze CPU that is in charge of slow-speed processes such as:
  - Forwarding tables maintenance:
    - Add new entries by monitoring ARP transactions.
    - Remove old entries based on timer mechanism.
  - IGMP snooping and multicast tables maintenance.
  - Link status and control.
  - Management agent implementation (SNMP) and MIB maintenance.
  - Time synchronization support (IEEE 1588) with help from hardware.
  - GPS module interface and control.
- Packet buffers are implemented on external DRAM modules.

IEEE 1588 Support

- **Grandmaster Clock**: the switch acts as the grandmaster in the IEEE 1588 protocol and precision timing is based on a GPS-disciplined 10MHz clock with less than 5 parts per trillion frequency stability and holdover stability under 20us over a 3-hour period.
- **IEEE 1588 Controller**: Sits in the PSE and has direct access to packets for sync. accuracy. Synchronization is achieved through the exchange of few UDP packets.



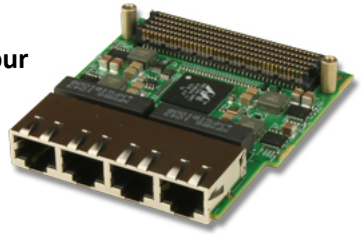


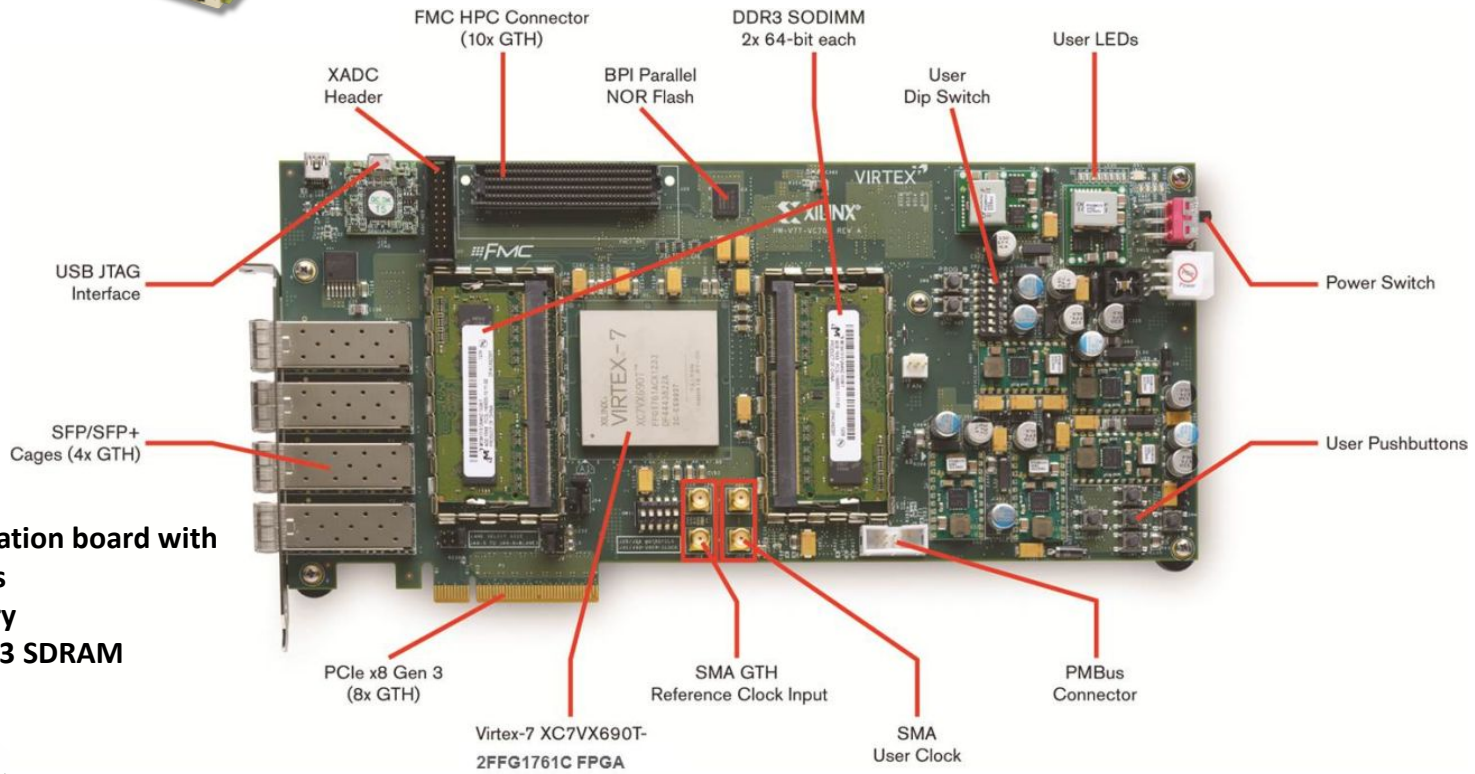
Phase I Overview

- During Phase I, we focused on the development of the FPGA firmware on a COTS hardware to ensure the correct functionality of our design, and designed and developed the following components:
  - Layer 2 switch engine (MAC address based switching).
  - Layer 3 switch engine (IPv4 address based switching and support for IGMP).
  - Both engine are non-blocking.
  - IEEE 1588 engine with grandmaster clock (design only).
- 1G subsystems was fully tested with Spirent test tools.
- 10G subsystem was partially tested with IXIA test tools.

Phase I COTS Hardware

FMC expansion board with four 10/100/1000 ports.





VC709 Virtex-7 FPGA evaluation board with

- **4 fiber 10GBase-SR ports**
- **128MB of FLASH memory**
- **2 independent 4GB DDR3 SDRAM**

Phase I COTS Hardware

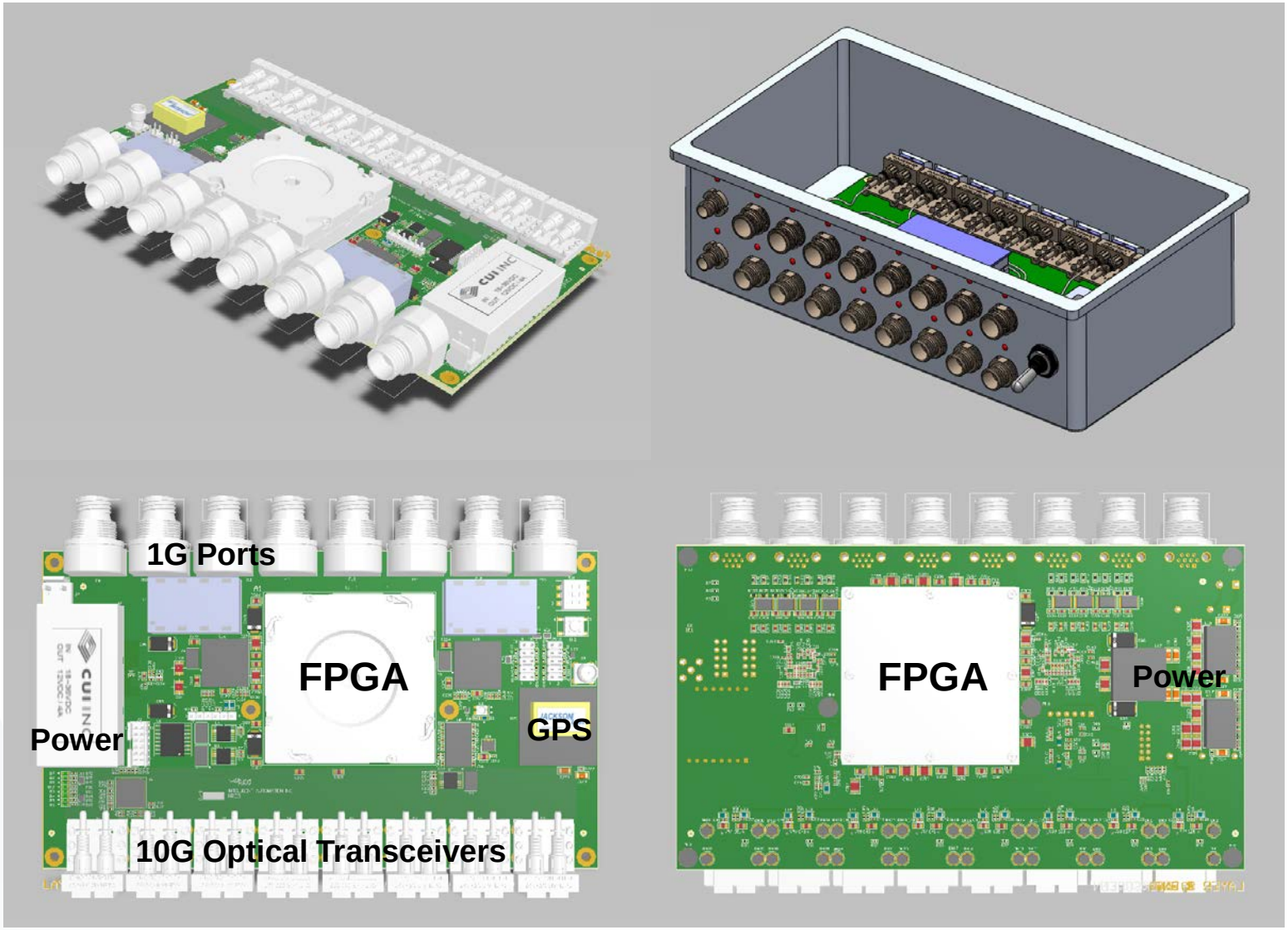
Phase I Results

- In the Phase I final briefing, all 1G ports were tested using a Spirent SmartBits 600B Network Performance Analyzer tool:
  - Non-Blocking: Spirent SmartFlow tool was used to generate layer 3 traffic at line rate on all four ports. The results showed no packet drops, and latency of 2.4uS to 3.4us in each port.
  - Multicast: using SmartFlow we defined 400 multicast addresses and ran a multicast test were packet from one port were generated at 100% load to all other ports in a multicast fashion. Again, no packet drops were observed.
- 10G ports were tested using IXIA 10G testbed, two ports at a time.
  - Layer 2/3 traffic was generated at line rate on both ports. The results showed no packet drops, and latency of less than 1us.

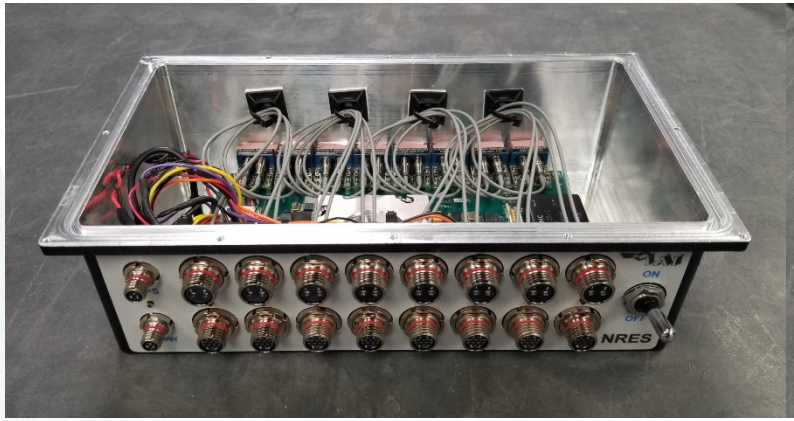
Phase II Overview

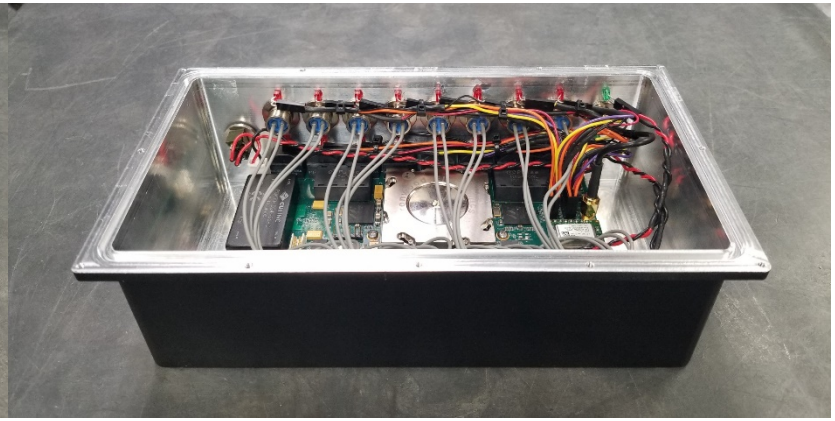
- We improved the FPGA firmware on the COTS hardware, specifically:
  - Time synchronization (IEEE 1588 engine) added.
  - Management support (SNMP with partial MIB) added.
  - Number of ports increased to 16 (in progress).
  - FPGA device upgraded (in progress).
- We are developing a ruggedized and miniaturized board suitable for airborne applications.
  - Schematic and PCB design completed.
  - Fabrication and assembly is completed.
  - Testing is in progress.
- Expected end date is June 2018.

Phase II Hardware



Phase II Hardware





Phase II Tests

- To maintain cost, we tested NRES with in-house testing tools.
- We used our Phase I COTS hardware to generate Ethernet packet on four ports at a time and verify the results.
- We used following standards to generate traffic:
  - RFC 2889 for layer 2
  - RFC 2544 for layer 3
  - RFC 3918 for Multicast
- Packets are generated with unique IDs and the ID was captured and stored on the receiving port.

- Standard test with Spirent test tools will be conducted upon delivery to TRMC SET personnel.

Summary and Conclusions

- NRES is a managed ruggedized Ethernet switch with support for eight 10G and eight 1G ports, and guarantees non-blocking functionality at full line rate.
- NRES acts as a grandmaster clock and timing source for the telemetry network through GPS-linked timing unit.
- The preliminary COTS based prototype has been validated with Spirent and IXIA test tools (full 1G and partial 10G).
- The ruggedization and miniaturization of NRES is completed.
- Final NRES switch has been tested and verified with in-house test tools.
- Complete tests with standardized test tools will be performed at Edwards at delivery.

Acknowledgements

- IAI would like to thank the following people for their technical, contractual and managerial support during this project:
  - Tom Young
  - Benjamin Tomlinson
  - Mark Radke
  - Mark Santiago
  - Thomas O'Brien
  - Peter Weed
  - Michael Thomasson
  - Marnita Harris
  - Antoniette Karnitz
  - Robert Palmer

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	**2. REPORT TYPE**	**3. DATES COVERED** *(From - To)*
10/05/2019	Briefing slides	May 14-16, 2019, ITEA, Las Vegas.

4. TITLE AND SUBTITLE
NRES: Non-blocking Ruggedized Ethernet Switch for Airborne Applications

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Dr. Ali Namazi, Dr. Chujen Lin

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) AND ADDRESS(ES)
Intelligent Automation, Inc.
15400 Calhoun Dr., Suite 190,
Rockville, MD-20855

8. PERFORMING ORGANIZATION REPORT NUMBER
412TW-PA-19264

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
412th Test Wing
195 E Popson Ave
Edwards AFB CA 93524

10. SPONSOR/MONITOR'S ACRONYM(S)
N/A

11. SPONSOR/MONITOR'S REPORT NUMBER(S)

12. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release A: distribution is unlimited.

13. SUPPLEMENTARY NOTES
ITEA, Las Vegas, Nevada, United States, May 14-16, 2019

14. ABSTRACT
Telemetry communication and its transport/routing protocols are based on Ethernet standards. A key element of the network infrastructure is the Ethernet switch, which is the critical junction point of all devices on the network. Current ruggedized Ethernet switches do not support non-blocking solutions at 10Gbps speeds. To address the gap, IAI is developing an FPGA-based (Field programmable Gate Array) ruggedized Ethernet switch (NRES) that is true non-blocking and ruggedized with support for several 10Gbps ports and 10/100/1000 ports.

15. SUBJECT TERMS
Ethernet switch, ruggedized, non-blocking, FPGA, IEEE 1588

16. SECURITY CLASSIFICATION OF:			**17. LIMITATION OF ABSTRACT**	**18. NUMBER OF PAGES**	**19a. NAME OF RESPONSIBLE PERSON**
Unclassified					412 TENG/EN (Tech Pubs)
a. REPORT	**b. ABSTRACT**	**c. THIS PAGE**	None	21	**19b. TELEPHONE NUMBER** *(include area code)*
Unclassified	Unclassified	Unclassified			661-277-8615